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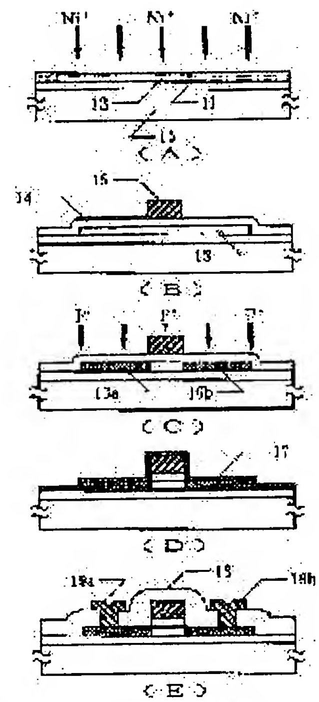
(54) THIN FILM TRANSISTOR AND PREPARATION THEREOF

(57)Abstract:
PURPOSE: To improve throughput by making an active region of a crystalline silicon film formed on a substrate have a catalytic element promoting more than specific crystallization and making concentration of a catalytic element of an impurity region adjacent to the active region larger than that of the active region.
CONSTITUTION: A foundation film 11 of silicon oxide is formed on a substrate 10 by sputtering. Next, an amorphous silicon film is piled up to crystallize. Later, the silicon film is patterned so as to form an insular silicon region 12. Further, a silicon oxide film 14 is piled up as a gate insulating film. Then, the silicon film is patterned so as to form a gate electrode 15. Next, the silicon oxide film 14 is etched so as to activate the impurity regions 16a, 16b to crystallize. At this time, a catalytic element for crystallization is made to have larger concentration than the concentration 1×1011cm of the active region of a crystalline silicon film. Thereby, crystallization time can be shortened.



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CLAIMS

[Claim(s)]
[Claim 1] The concentration of the catalyst element of the impurity range which has the active region of the crystalline silicon film formed on the substrate, has the catalyst element which promotes three or more [1x1017cm -] crystallization in the active region, and adjoins the aforementioned active region is TFT characterized by being larger than the thing of the aforementioned active region.
[Claim 2] It is the TFT characterized by a catalyst element being at least one of nickel, iron, cobalt, and the platinum in a claim 1.
[Claim 3] It is the TFT characterized by being the value by which the concentration of a catalyst element was measured with the secondary ion mass spectrometry in the claim 1.
[Claim 4] The production method of TFT characterized by providing the following. The 1st process at which the concentration of a catalyst element forms less than [1x1017cm -] three amorphous silicon film on a substrate. The 2nd process which adds the catalyst element which promotes crystallization on the aforementioned amorphous silicon film. The 3rd process which forms a gate electrode on the aforementioned silicon film. The 4th process which introduces a doping impurity into the aforementioned silicon film by using the aforementioned gate electrode as a mask, the 5th process which forms the matter which sticks to the aforementioned silicon film and has a catalyst element, and the 6th process which activates the impurity introduced by carrying out heat annealing of the aforementioned silicon film.
[Claim 5] It is the production method of the TFT characterized by the bird clapper from the process combined thermally after sticking the material into which the 2nd process has a catalyst element in a claim 4 to an amorphous silicon.
[Claim 6] The production method of the TFT characterized by the material which has a catalyst element being the compound of a catalyst element and silicon in a claim 5.
[Claim 7] The production method of TFT characterized by providing the following. The 1st process at which the concentration of a catalyst element forms less than [1x1017cm -] three amorphous silicon film on a substrate. The 2nd process which adds the catalyst element which promotes crystallization on the aforementioned amorphous silicon film. The 3rd process which forms a gate electrode on the aforementioned silicon film. The 4th process which introduces a doping impurity and the catalyst element of three or more [1x1017cm -] concentration into the aforementioned silicon film by using the aforementioned gate electrode as a mask, and the 5th process which activates the impurity introduced by carrying out heat annealing of the aforementioned silicon film.
[Claim 8] The production method of TFT characterized by providing the following. The 1st process at which the concentration of a catalyst element forms three or more [1x1017cm -] amorphous silicon films on a substrate. It is a maximum temperature T1 about the aforementioned amorphous silicon film. The 2nd process which anneals. The 3rd process which forms a gate electrode on the aforementioned silicon film. The 4th process which introduces a doping impurity and a catalyst element into the aforementioned silicon film by using the aforementioned gate electrode as a mask, and the 5th process which activates the impurity introduced by annealing the aforementioned silicon film by the maximum temperature T2 (<T1).
[Claim 9] The production method of the TFT characterized by being T1-T2 >50 degree C in a claim 6.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to TFT (TFT) and its production method. The TFT produced by this invention is formed in all on semiconductor substrates, such as single crystal silicon, on insulating substrates, such as glass. Especially this invention relates to the TFT produced through crystallization by heat annealing, and activation.
[0002]
[Description of the Prior Art] Recently, the research of an insulated-gate type semiconductor device which has a thin film-like barrier layer (it is also called an active region) on an insulating substrate is made. Especially, a thin film-like insulated gate transistor and the so-called TFT (TFT) are studied eagerly. These are formed on a transparent insulating substrate, and in display, such as liquid crystal which has matrix structure, it is the purpose to use for to use for control of each pixel or a drive circuit, and they are distinguished by the material and the crystallized state of the semiconductor to be used like an amorphous silicon TFT and crystalline silicon TFT.
[0003] Generally, the electric-field mobility of the semiconductor of an amorphous state is small, therefore cannot be used for TFT as which high-speed operation is required. Moreover, in an amorphous silicon, since the electric-field mobility of P type is remarkably small, P channel type TFT (TFT of PMOS) cannot be produced, therefore the MOS circuit (CMOS) of a complementary type cannot be formed combining N channel type TFT (TFT of NMOS).
[0004] On the other hand, a crystal semiconductor has electric-field mobility larger than an amorphous semiconductor, therefore high-speed operation is possible for it. Since not only TFT of NMOS but TFT of PMOS is obtained similarly, it is possible to form a CMOS circuit, for example, in the liquid crystal display of an active matrix, what has the so-called monolithic structure which constitutes not only an active-matrix portion but circumference circuits (driver etc.) from crystallinity TFT of CMOS is known for crystalline silicon. Since it is such, research and development of TFT which used crystalline silicon are prosperous recently.
[0005]
[Problem(s) to be Solved by the Invention] Although the method of crystallizing an amorphous silicon by irradiating laser or a strong light equivalent to it as one of the methods which obtains crystalline silicon is mentioned, mass-production utilization is not in prospect for the instability of the output of laser, or the instability originating in being a short-time process very much.
[0006] The method employable practical now considered is a method of crystallizing an amorphous silicon with heat. By this method, crystal silicon with little dispersion between batches can be obtained. However, it is necessarily satisfactory.
[0007] usually, crystalline silicon -- obtaining -- prolonged annealing with a temperature of about 600 degrees C -- or annealing 1000 degrees C or more in an elevated temperature was required The substrate which can be chosen if the latter method is adopted was restricted to the quartz, and substrate cost became very high. Although the room of substrate selection spreads by the former method, there is another problem.
[0008] The production processes of the conventional TFT at the time of adopting cheap alkali-free-glass substrates, such as Corning(, Inc. etc.) of No. 7059, are the in general following flows.
** Crystallization of the membrane formation ** amorphous silicon film of an amorphous silicon film (600 degrees C or more, 24 hours or more)
** Introduction of the formation ** doping impurity of the membrane formation ** gate electrode of a gate insulator layer (based on an ion implantation or the ion doping method)
** Activation of a doping impurity (600 degrees C or more, 24 hours or more)
** Formation of the formation ** source of a layer insulation object, and a drain electrode [0009] Here, the process of ** and ** poses especially a problem. Since the distortion temperature of many alkali free glasses is nearly (it is 593 degrees C when it is Corning 7059) 600 degrees C, processing at such temperature poses shrinkage of a substrate and a problem of a camber. Since patterning is not carried out yet in the stage of ** which is the first annealing process, contraction of a substrate is in so big a problem among an oak, and it is **. However, in the stage of **, since patterning of a circuit is carried out, if a substrate contracts, future mask ****** will become impossible and it will become the big cause of a fall of the yield. Then, while to perform process temperature of ** below at the distortion temperature of a substrate is desired, to perform the process of ** more at low temperature (50-degree-C or more low temperature, still more preferably than distortion temperature [Preferably] of glass the highest heat treatment temperature of ** 50-degree-C or more low temperature) is desired.
[0010] For that purpose, although the method using the above laser etc. was also considered for example, in addition to the

instability of laser, stress occurred from the difference in a temperature rise between the portion (the source, drain field) by which laser is irradiated, and the portion (field under an active-region = gate electrode) by which laser is not irradiated, and it was observed that reliability falls.
[0011] For this reason, it was difficult in mass production to adopt laser etc. On the other hand, the present condition was being unable to find out the effective method as the other methods. such [this invention] a difficult technical problem -- receiving -- an answer -- it is going to give -- it is a thing this invention makes it a technical problem to solve the above-mentioned trouble, maintaining mass-production nature.
[0012]
[Means for Solving the Problem] As a result of research of this invention person, by adding the catalyst material of a minute amount on the silicon coat of an amorphous state substantially, crystallization was promoted, crystallization temperature was reduced and it became clear that crystallization time can be shortened. As a catalyst material, compounds, such as nickel (nickel), iron (Fe), cobalt (Co), simple substances of platinum (Pt), or those silicides, are suitable. The film which has these catalyst elements, a particle, a cluster, etc. can specifically be stuck and formed in the bottom of an amorphous silicon film, or a top, or these catalyst elements can be introduced into an amorphous silicon film by methods, such as ion-implantation, and this can be crystallized after that suitable temperature and by carrying out heat annealing at the temperature of 580 degrees C or less typically.
[0013] Although it is natural, crystallization time has the relation of being short, so that an annealing temperature is high. Moreover, crystallization temperature is so low that the concentration of nickel, iron, cobalt, and platinum is large, and there is a relation that crystallization time is short. In research of this invention people, in order to have advanced crystallization, it turns out that it is required for the 5x1018cm - 3 more than concentration of at least one of elements of these to exist preferably three or more [1x1017cm -].
[0014] On the other hand, since each above-mentioned catalyst material is a material which is not desirable for silicon, it is desired for the concentration to be low as much as possible. Especially in research of this invention people, when using as an active region, in order to acquire sufficient reliability and a sufficient property, to total the concentration of such catalyst material and not to exceed 1020cm-3 is desired. On the other hand, even if it existed in the source and the drain comparatively so much, it became clear not to very become a problem.
[0015] This invention people found out that the above-mentioned problem was solvable by using this paying attention to the effect of this catalyst element. The production process of TFT in this invention is in general as follows.
** Introduction of the membrane formation **' catalyst element of an amorphous silicon film (based on an ion implantation or the ion doping method)
** Crystallization of an amorphous silicon film (600 degrees C or less, less than 8 hours)
** Introduction of the formation ** doping impurity of the membrane formation ** gate electrode of a gate insulator layer (based on an ion implantation or the ion doping method)
** Activation of the membrane formation ** doping impurity to the silicon film of the matter which has 'catalyst element (600 degrees C or less, less than 8 hours)
** Formation of the formation ** source of a layer insulation object, and a drain electrode [0016] Or introduction of the membrane formation **' catalyst element of a ** amorphous silicon film (based on an ion implantation or the ion doping method)
** Crystallization of an amorphous silicon film (600 degrees C or less, less than 8 hours)
** Introduction of the formation ** doping impurity of the membrane formation ** gate electrode of a gate insulator layer (based on an ion implantation or the ion doping method)
** Introduction of 'catalyst element (based on an ion implantation or the ion doping method)
** Activation of a doping impurity (600 degrees C or less, less than 8 hours)
** Formation of the formation ** source of a layer insulation object, and a drain electrode [0017] In these processes, ** and **' can also reverse the sequence. Moreover, you may transpose the process of **' to "the process which sticks the coat which has a catalyst element on an amorphous silicon film or to the bottom." Although meanses, such as ion-implantation from the meaning of controlling the concentration of a catalyst element precisely, are desirable, a process is simplified, and from a viewpoint of suppressing plant-and-equipment investment, as long as the property of TFT obtained allows, you may adopt such a process.
[0018] In this invention, the catalyst element which the catalyst element introduced into the amorphous silicon film by above-mentioned process **' made promote the crystallization remarkably, and was mainly introduced into the source and the drain field by **' promotes the recrystallization of the field remarkably. Therefore, for crystallization and activation, the temperature of 550 degrees C or less is typically enough, and 600 degrees C or less also of annealing time are also typically enough in less than 4 hours for less than 8 hours. When the catalyst element is especially distributed from the beginning equally by ion-implantation or the ion doping method, crystallization tended [very] to advance.
[0019] In this invention, even if it adopts which process, since a gate electrode exists on an active region, a catalyst element sticks to an active region direct at the process of **', or it is not poured in. Therefore, it is possible to change the concentration of a catalyst element in an active region and an impurity range. For example, by making comparatively small concentration of the catalyst element added by the active region, by enlarging comparatively concentration of the catalyst element which lessens the bad influence which it has on the property and reliability of TFT as much as possible, and is added by the impurity range, and reducing the temperature of activation, contraction and the camber of a substrate can be suppressed and the yield can be raised. Moreover, for the reason, the reliability of TFT and a property are not almost spoiled.
[0020] Furthermore, in this invention, the thin amorphous silicon film 1000A or less which is not crystallized for an operation of

a catalyst element is also crystallized depending on the usual heat annealing. From a viewpoint which prevents the pinhole of the gate insulator layer in the level difference section of TFT, an open circuit of poor insulation and a gate electrode, etc., as for the thickness of a crystal silicon film, 500A or less 1000A or less was demanded preferably. Although it was unrealizable by any methods other than laser crystallization, also in low temperature, it was [with this invention] conventionally realizable with heat annealing. It cannot be overemphasized that this contributes to the further improvement in the yield. An example is used for below and this invention is explained more to a detail.

[0021]

[Example]

[Example 1] The cross section of the production process of this example is shown in drawing 1 . First, the ground film 11 of oxidization silicon with a thickness of 2000A was formed by the sputtering method on the substrate (Corning 7059) 10. Furthermore, 500-1500A in thickness and the 1500A intrinsic (I type) amorphous silicon film 12 were deposited by the plasma CVD method. And nickel ion was poured into this amorphous silicon film with ion-implantation by the dose of 1x1013-5x1014cm-2, 5x1013cm-2 [for example,]. Consequently, in the amorphous silicon film, nickel existed by about 5x1018cm -] three concentration. (Drawing 1 (A))

[0022] Among nitrogen-gas-atmosphere mind, at 550 degrees C, this was annealed for 4 hours and crystallized. Patterning of the silicon film was carried out after annealing, the island-like silicon field 13 was formed, and the oxidization silicon film 14 with a thickness of 1000A was further deposited as a gate insulator layer by the sputtering method. Using oxidization silicon as a target, the substrate temperature at the time of sputtering is oxygen and an argon, and made 200-400 degrees C, for example, 250 degrees C, and sputtering atmosphere at sputtering an argon / oxygen =0-0.5 (0.1 or less [for example,]).

[0023] Then, 3000-8000A in thickness and the 6000A silicon film (0.1 - 2% of phosphorus is included) were deposited by reduced pressure CVD. In addition, as for the membrane formation process of this oxidization silicon and a silicon film, it is desirable to carry out continuously. And patterning of the silicon film was carried out and the gate electrode 15 was formed. (Drawing 1 (B))

[0024] Next, the impurity (phosphorus) was poured into the silicon field by using a gate electrode as a mask by the plasma doping method. Acceleration voltage was made into 60-90kV, for example, 80kV, using a phosphoretted hydrogen (PH3) as doping gas. The dose carried out to 1x1015-8x1015cm-2, 2x1015cm-2 [for example,]. Consequently, the impurity ranges 16a and 16b of N type were formed. (Drawing 1 (C))

[0025] Next, the oxidization silicon film 14 on an impurity range was **********ed, the impurity range 16 was exposed, and by the sputtering method, 5-200A in thickness and the 20A silicification nickel film (a chemical formula NiSix and 0.4<=x<=2.5, for example, x= 2.0) 17 were formed in the whole surface, as shown in drawing on the average. Although the modality of the aggregate of the grain child which a film is not continuous and it is was presented by the thickness of about 20A, it is satisfactory in this example. (Drawing 1 (D))

[0026] Then, the impurity was activated among nitrogen-gas-atmosphere mind by annealing for 4 hours at 480 degrees C (it being 70-degree-C low from the annealing temperature in the case of previous crystallization). Since nickel was spread from the silicification nickel film previously put on the N type impurity ranges 16a and 16b on it at this time, recrystallization advanced easily by this annealing. In this way, impurity ranges 16a and 16b were activated.

[0027] Then, it formed by the plasma CVD method by having used the oxidization silicon film 18 with a thickness of 6000A as the layer insulation object, the contact hole was formed in this, and the electrode and the wiring 19a and 19b of the source field of TFT and a drain field were formed by the multilayer of a metallic material, for example, a titanium nitride, and aluminum. Finally, 350 degrees C and annealing for 30 minutes were performed in the hydrogen atmosphere of one atmospheric pressure. TFT was completed according to the above process. (Drawing 1 (E))

[0028] When the concentration of the nickel in the active region (under a gate electrode) of obtained TFT was analyzed by the secondary ion mass analysis (SIMS) method, it was about [1x1018 to 5x1018cm -] three, and the concentration in an impurity range 16 was about [1x1019 to 5x1019cm -] three.

[0029] [Example 2] The cross section of the production process of this example is shown in drawing 2 . First, the ground film 21 of oxidization silicon with a thickness of 2000A was formed by the sputtering method on the substrate (Corning 7059) 20. Furthermore, 500-1500A in thickness, the 1500A intrinsic (I mold) amorphous silicon film 22, and the oxidization silicon film 23 that is 200A in thickness by the sputtering method further were deposited by the plasma CVD method. And nickel ion was poured into this amorphous silicon film by the dose of 5x1013cm-2 with ion-implantation. (Drawing 2 (A)) Next, among nitrogen-gas-atmosphere mind, 550 degrees C, this amorphous silicon film was annealed for 8 hours, and was crystallized. Then, patterning of this silicon film was carried out, and the island-like silicon field 24 was formed.

[0030] Furthermore, oxidization silicon 25 with a thickness of 1000A was formed as a gate insulator layer of crystal silicon TFT by the plasma CVD method by using a tetrapod ethoxy silane (Si (OC two H5)4, TEOS) and oxygen as a raw material. In addition to the above-mentioned gas, the trichloroethylene (C2 HCl3) was used for the raw material. Before membrane formation, oxygen was passed 400 SCCMs to the chamber, plasma was generated in the substrate temperature of 300 degrees C, the total pressure of 5Pa, and RF power 150W, and this state was maintained for 10 minutes. Then, 15SCCM(s) were introduced for oxygen 300SCCM and TEOS, 2SCCM(s) were introduced into the chamber for the trichloroethylene, and the oxidization silicon film was formed. Substrate temperature, RF power, and total pressure were 300 degrees C, 75W, and 5Pa, respectively. The hydrogen of 100Torr(s) was introduced into the chamber after the completion of membrane formation, and hydrogen annealing for 35 minutes was performed at 350 degrees C.

[0031] Then, 3000-8000A in thickness and the 6000A tantalum film were deposited by the sputtering method. Titanium, a

tungsten, molybdenum, and silicon are sufficient instead of a tantalum. However, only the thermal resistance which can be equal to next activation is required. In addition, as for the membrane formation process of this oxidization silicon 25 and a tantalum film, it is desirable to carry out continuously. And patterning of the tantalum film was carried out and the gate electrode 26 of TFT was formed. Furthermore, the front face of this tantalum wiring was anodized and the oxide layer 27 was formed in the front face. Anodic oxidation was performed in 1 - 5% ethylene glycol solution of a tartaric acid. The thickness of the obtained oxide layer was 2000A. (Drawing 2 (B))

[0032] Next, the impurity (phosphorus) was poured into the silicon field by using a gate electrode as a mask by the plasma doping method. Acceleration voltage was set to 80kV, using a phosphoretted hydrogen (PH3) as doping gas. The dose was set to 2x1015cm-2. Consequently, the impurity ranges 28a and 28b of N type were formed. At this time, the gate electrode 26 and the impurity range 28 are in the offset state for the anodic oxidation object. (Drawing 2 (C))

[0033] Furthermore, nickel ion was poured into the silicon field by using a gate electrode as a mask with the ion implantation this time. The dose carried out to 1x1014-2x1015cm-2, 5x1014cm-2 [for example,]. Consequently, the concentration of the nickel of the impurity ranges 28a and 28b of N type became about [5x1019cm -] three. (Drawing 2 (D))

[0034] Then, the impurity was activated by annealing at 450 degrees C for 4 hours among nitrogen-gas-atmosphere mind. Since nickel ion was poured into the N type impurity ranges 28a and 28b at this time, recrystallization advanced easily by this annealing. In this way, impurity ranges 28a and 28b were activated.

[0035] Then, the oxidization silicon film 29 with a thickness of 2000A was formed as a layer insulation object by the plasma CVD method which uses TEOS as a raw material, the contact hole was formed in this, and the source, a drain electrode, and Wiring 30a and 30b were formed by the multilayer of a metallic material, for example, a titanium nitride, and aluminum. The semiconductor circuit was completed according to the above process. (Drawing 2 (E))

[0036] The leakage current when, as for the electric field effect mobility of the produced TFT, 70-100cm2 / Vs is impressed to 2.5-4.0V, and a gate and a threshold impresses the voltage of -20V to them by gate-voltage 10V was below 10-13 A.

[0037]

[Effect of the Invention] this invention can raise a throughput by activating crystallization of an amorphous silicon, and the doping impurity in silicon in low temperature, such as 400-550 degrees C, and a short time of 4 hours. In addition, although the shrinkage of a glass substrate had become a problem as a cause of a yield fall when a process 600 degrees C or more was adopted conventionally, such a trouble was cancelable at a stretch by using this invention.

[0038] This means that the substrate of a large area can be processed at once. That is, a unit price can be sharply reduced by cutting down many semiconductor circuits (matrix circuit etc.) from one substrate by processing a large area substrate. When this is applied to a liquid crystal display, improvement in mass-production nature and an improvement of a property are achieved. Thus, this invention is useful invention on industry.

[Translation done.]

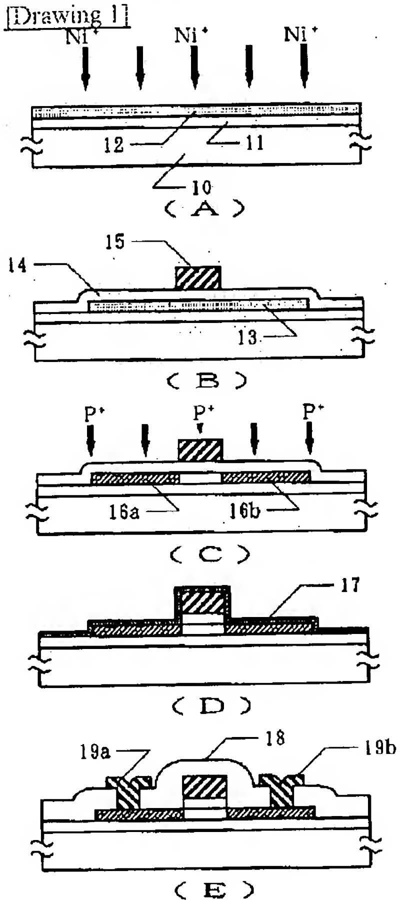
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The production process cross section of an example 1 is shown.
[Drawing 2] The production process cross section of an example 2 is shown.
[Description of Notations]
10 ... Substrate
11 ... Ground insulator layer (oxidization silicon)
12 ... Amorphous silicon film
13 ... Island-like silicon field
14 ... Gate insulator layer (oxidization silicon)
15 ... Gate electrode (silicon by which the phosphorus dope was carried out)
16 ... The source, drain field
17 ... Coat containing the catalyst element (silicification nickel)
18 ... Layer insulation object (oxidization silicon)
19 ... Metal wiring and electrode (a titanium nitride/aluminum)

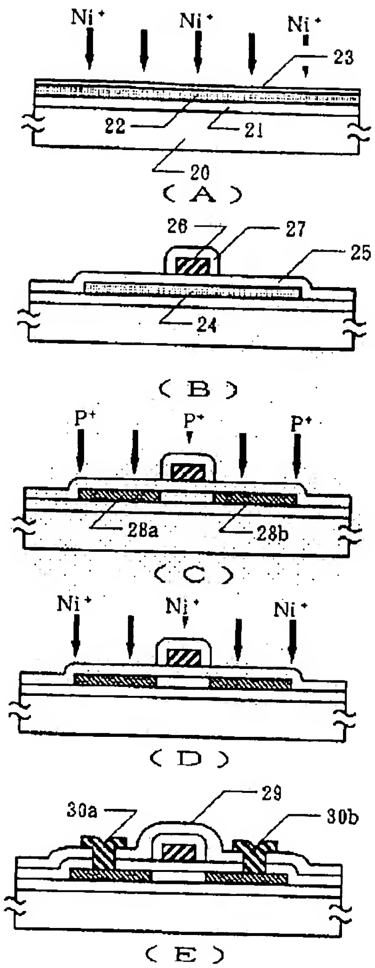
[Translation done.]

DRAWINGS

[Drawing 1]



[Drawing 2]



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